

F I G. 1

Test Vector \ Fault	f_1	f_2	f_3	f_4	f_5	f_6	f_7	f_8	f_9	f_{10}	f_{11}	f_{12}
t_1	X	X		X			X					
t_2	X		X	X					X			
t_3		X			X		X				X	
t_4			X			X						
t_5				X						X		
t_6				X			X	X	X			X
t_7					X		X	X				X

FIG. 2

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Test Vector	Fault Vector	f_1	f_3
t_1		X	
t_2		X	X
t_4			X

FIG. 3

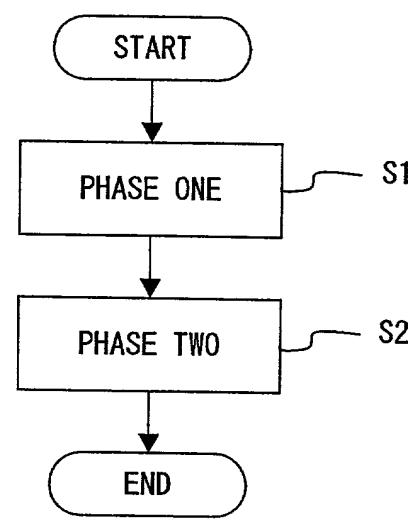
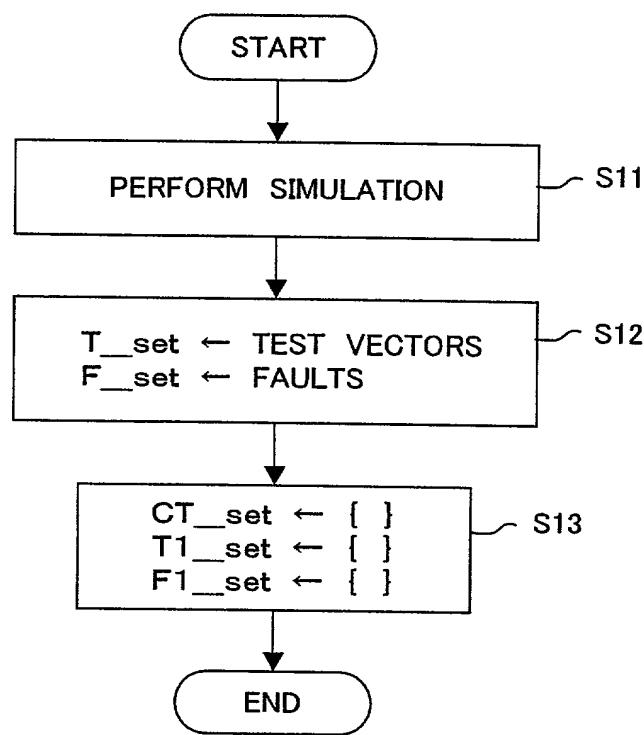


FIG. 4



F I G. 5

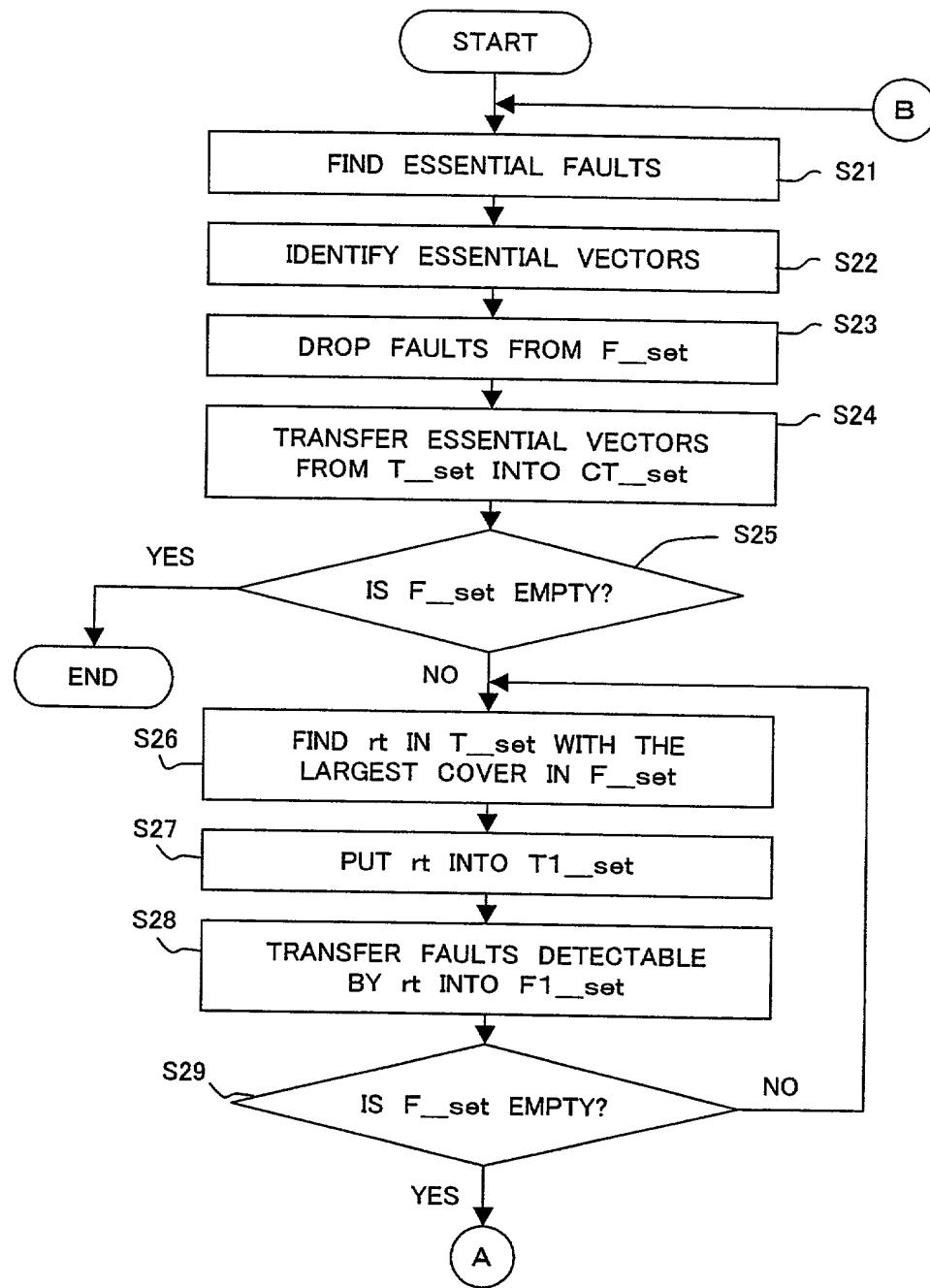
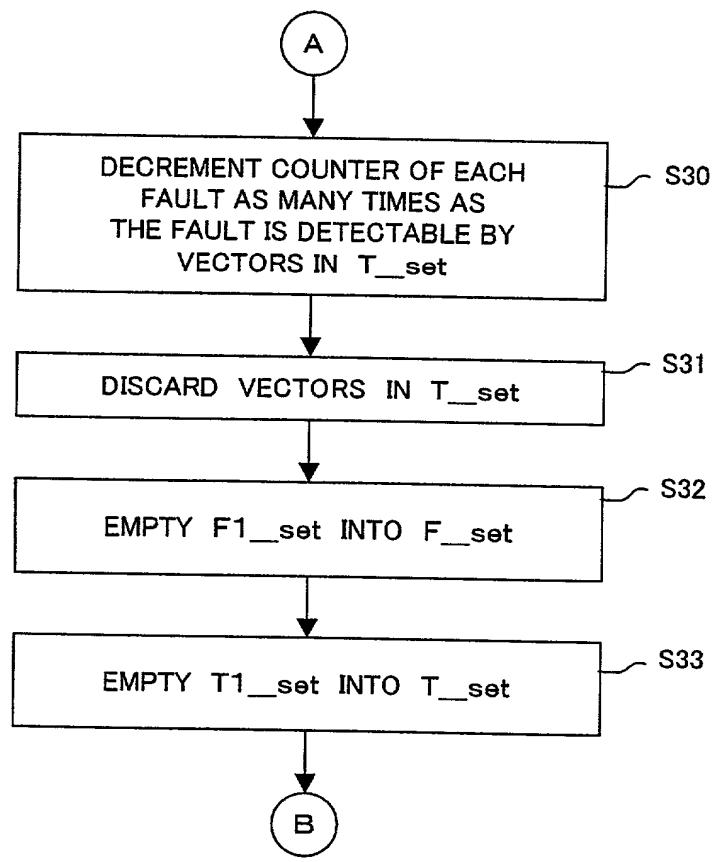
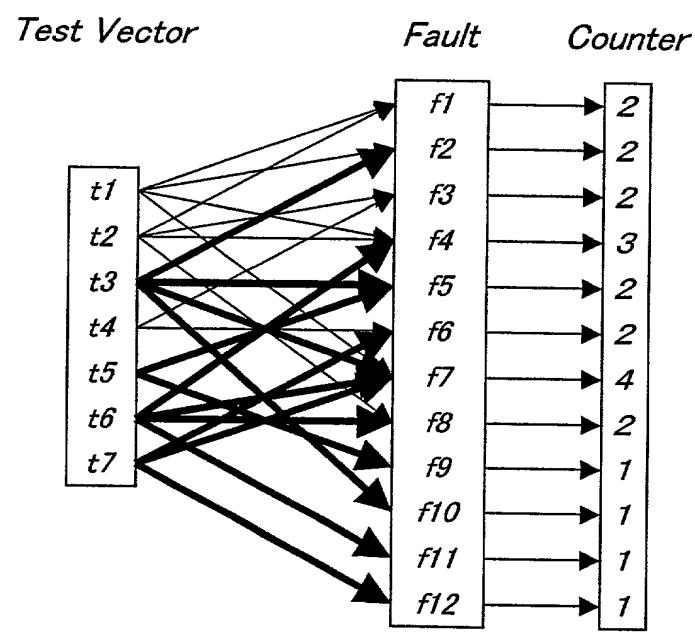


FIG. 6



F I G. 7



F I G. 8

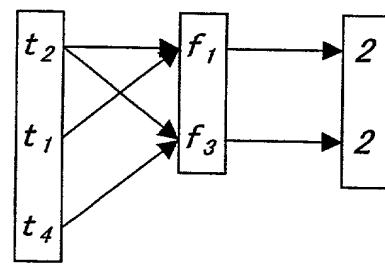


FIG. 9

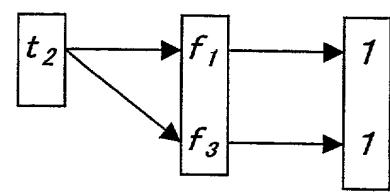


FIG. 10

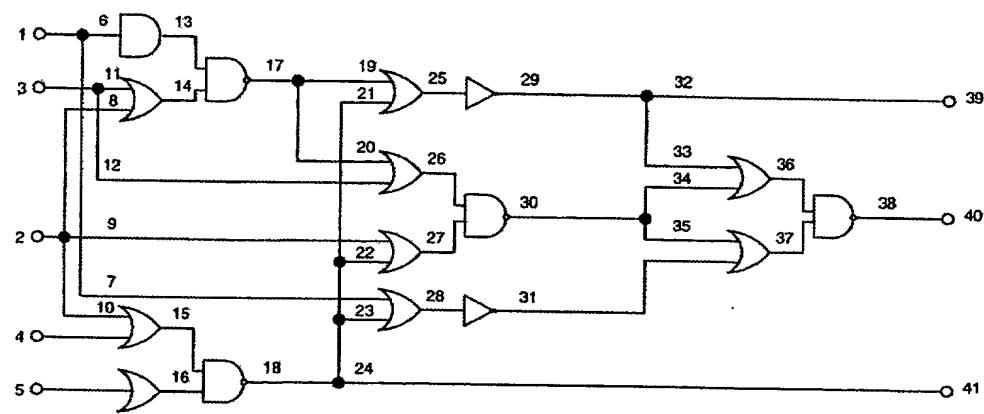


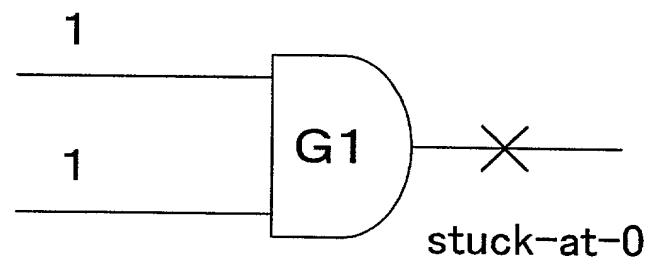
FIG. 11

Test Vector	Pattern
t_1	0 1 2 2 1
t_2	1 1 2 2 1
t_3	2 0 2 0 1
t_4	2 1 2 0 1
t_5	1 0 0 1 1
t_6	1 0 1 1 1
t_7	2 0 2 1 1
t_8	2 1 2 2 0
t_9	2 1 2 2 1
t_{10}	1 0 0 1 0
t_{11}	1 1 0 1 1
t_{12}	0 0 1 1 1
t_{13}	0 1 1 1 1
t_{14}	1 1 0 2 1
t_{15}	1 1 1 2 1
t_{16}	0 1 0 2 0

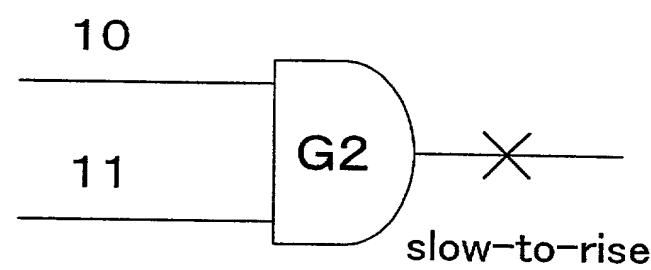
F I G. 12

Fault	Counter	Test Vector	#Fault
1/1	3	t_1	6
5/1	3	t_2	0
6/1	3	t_7	0
8/0	2	t_8	2
12/1	2	t_9	0
13/1	3	t_{10}	2
16/1	3	t_{11}	4
20/1	2	t_{12}	3
26/1	2	t_{13}	6
33/1	2	t_{14}	4
34/1	2	t_{16}	2
36/1	2		

F I G. 13



F I G. 1 4



F I G. 15

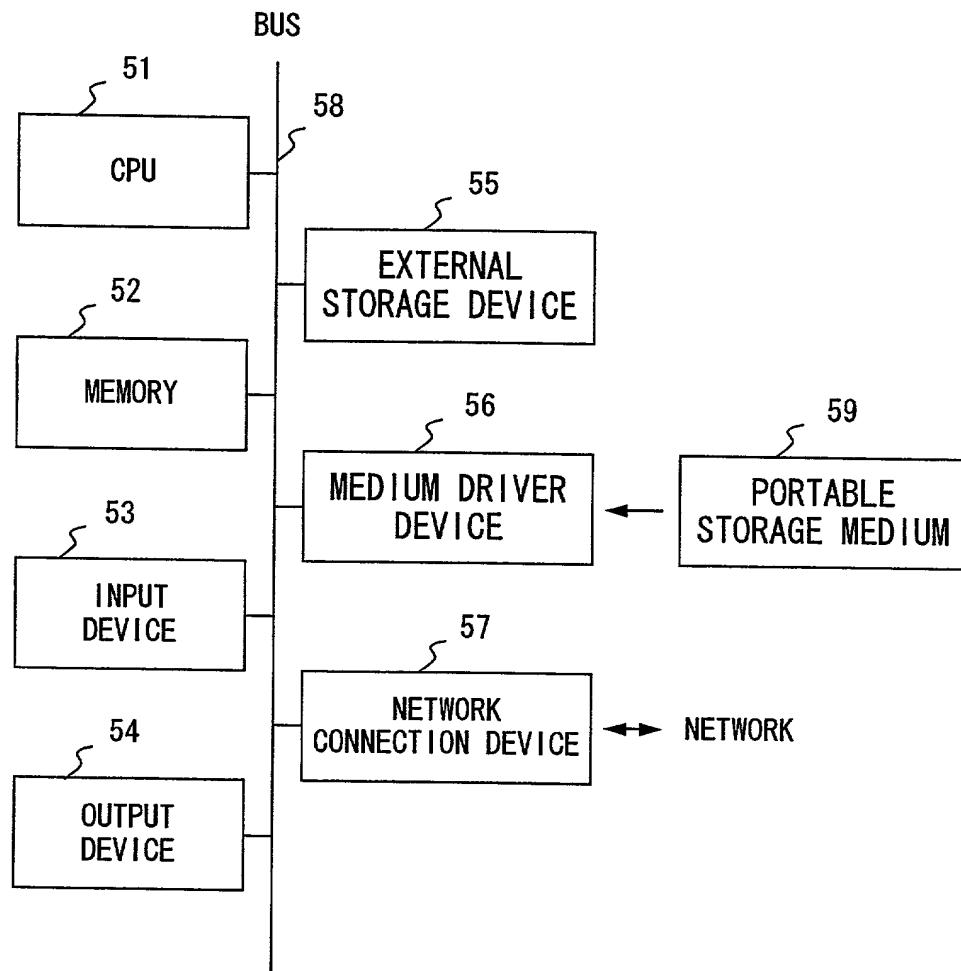
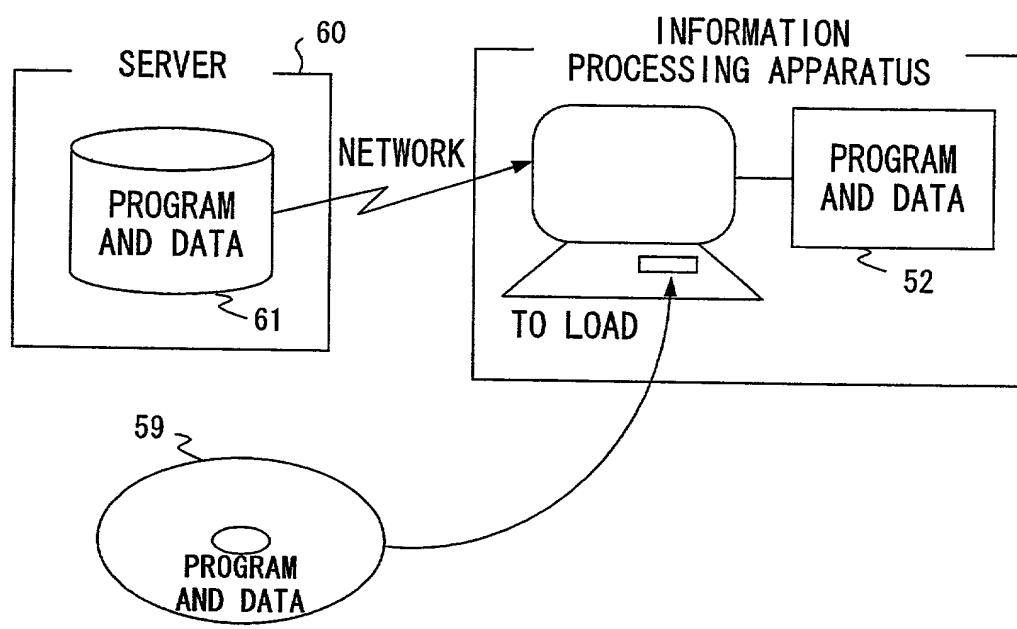


FIG. 16



F I G. 17